Electronic Version
Stylesheet Version v1.1.1

Description

[METHOD OF FORMING CONTACT OPENING AND METHOD OF FORMING SEMICONDUCTOR DEVICE]

Cross Reference to Related Applications

[0001] This application claims the priority benefit of Taiwan application serial no. 92116356, filed June 17, 2003.

Background of Invention

[0002] Field of the Invention

[0003] The present invention generally relates to a process of manufacturing semiconductor devices. More particularly, the present invention relates to a method of forming contact openings and a method of forming semiconductor devices.

[0004] Description of the Related Art

[0005] With rapid advancement in semiconductor fabrication technologies, the size of semiconductor devices has shrunk to deep sub-micron levels. As the level of integra-

tion of integrated circuits increases, the surface of a chip alone can hardly have sufficient area for accommodating all the interconnects. To provide necessary interconnects after device miniaturization, a design having two or more metallic interconnects is routinely used in very large scale integration (VLSI) packages. However, to connect two metallic lines at different layers, the intermediate insulating layer is bored to produce an opening and then a conductive material is deposited into the opening to form a conductive plug structure.

[0006] To combat the shrinking line width and prevent any misalignment of contact opening, most semiconductor devices employs a self-align contact design. This is particularly true in the design of a memory device. Typically, the doped region in a substrate and a bitline above the substrate are electrically connected through a self-aligned contact.

[0007] Figs. 1A through 1F are schematic cross-sectional views showing the progression of steps for producing a conventional contact opening in a memory device. As shown in Fig. 1A, a substrate 100 having a gate structure 112 with a cap layer 110 thereon is provided. Each gate structure 112 comprises a gate dielectric layer 104, a polysilicon

layer 106 and a metal silicide layer 108. The labeled region 102 is a prescribed region for forming a bitline contact while the labeled region 103 is a prescribed region where no bitline contact is formed.

[0008] As shown in Fig. 1B, a tungsten silicide etching process is performed to remove a portion of the sidewall of the tungsten silicide layer 108. Thus, the tungsten silicide layer 108a form a recess on the sidewall to neighboring film layers.

[0009] As shown in Fig. 1C, a thermal oxidation operation is performed to form an oxide liner 114 on the sidewalls of the gate structure 112 and the exposed substrate 100 surface. Because a portion of the metal silicide layer108 on the sidewall has been removed, lateral extrusion caused by crystal growth on the metal silicide layer 108a can be avoided.

[0010] As shown in Fig. 1D, a photoresist layer 116 is formed over the substrate 100 covering the region 103. Thereafter, a sidewall oxidation layer etching operation is performed to reduce the thickness of the exposed oxide liner 114 and produce an oxide liner 114a. The purpose of reducing the thickness of the oxide liner 114 within the region 102 is to increase the width of the gap (opening) and

reduce the aspect ratio so that the process window in subsequent etching or depositing operation can be increased.

[0011] As shown in Fig. 1E, the photoresist layer 116 is removed. A spacer 118 is formed on the sidewall of the gate structure 112 and the cap layer 110, for example, by forming a silicon nitride layer (not shown) over the substrate 100 and then perform an anisotropic etching operation. However, during the anisotropic etching operation, a portion of the exposed oxide liner 114a or the entire exposed oxide liner 114a may be removed due to a reduced thickness within the region 102. In other words, a portion of the substrate 100 will be exposed.

[0012] As shown in Fig. 1F, an insulation layer 120 is formed over the substrate 100. Thereafter, photolithographic and etching processes are carried out to pattern the insulation layer 120 and form a self-aligned contact (SAC) opening 122 within the region 102 between two neighboring gate structures 112.

[0013] Even though a portion of the substrate 100 within the region 102 has been exposed however, it is to be noted that portions of the substrate 100 may not be exposed in each and every contact openings in the other regions (not

shown).The etching process of self-align contact opening directly etch through to substrate to ensure that portions of the substrate 100 are exposed within other contact openings,. However, this practice may cause over-etching of the substrate 100 leading to some structural damage as shown by the numeral 117 in FIG. 1F.

[0014] In general, the region in the substrate 100 marked as 117 is a doped region (not shown). Hence, damaging the region 117 may lead to junction leakage problems. To compensate for the damage in the substrate 100, an additional ion implantation has to be carried out so that the correct dopant concentration is restored. Therefore, the processing step is not only more complicated but may also intensify short channel effect.

SUMMARY OF INVENTION

[0015] Accordingly, one object of the present invention is to provide a method of forming a contact opening capable of reducing junction leakage resulting from a damaged substrate surface in a conventional bitline contact opening fabrication process.

[0016] A second object of this invention is to provide a method of forming a contact opening capable of reducing the complexity in fabricating a conventional bitline contact

opening.

[0017] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a method of forming a contact opening. First, a substrate having a plurality of conductive structures such as gate structures thereon is provided. An ion implantation is performed for implanting nitrogen ions at a slant angle into the sidewalls of the conductive structures. Alternatively, an ion implantation is performed for implanting oxygen or argon ions vertically into the substrate between the conductive structures. A metal silicide etching process can also be optionally carried out before or after the ion implantation so that a portion of the metal silicide attached to the sidewall of the gate structures is removed. Thereafter, a thermal treatment is carried out to form a liner layer on the sidewall of the conductive structure and the exposed substrate. The liner layer on the sidewall of the conductive structure has a thickness smaller than the liner layer on the substrate surface. A spacer is formed on each side of the conductive structure and then an insulation layer is formed over the substrate. The insulation layer is patterned to form a contact opening between two neighbor-

ing conductive structures.

[0018] This invention also provides a method of fabricating a semiconductor device. First, a substrate with a plurality of gate structures each having a cap layer thereon is provided. An ion implantation is performed implanting nitrogen ions at a slant angle into the sidewall of the gate structure and the cap layer. Alternatively, oxygen or argon ions are implanted vertically into the substrate between two neighboring conductive structures. A metal silicide etching process can also be carried out by option before or after the ion implantation so that a portion of the metal silicide attached to the sidewall of the gate structures is removed. Thereafter, a thermal treatment is carried out to form a liner layer on the sidewall of the conductive structure and the exposed substrate. The liner layer on the sidewall of the gate structure and the cap layer have a thickness smaller than the liner layer on the substrate surface.

[0019] This invention utilizes a tilted or a vertical ion implantation to reduce the thickness of the liner layer that is subsequently formed on the sidewall of a gate structure when compared with the liner layer on the substrate surface. Ultimately, a wider gap is produced between the neighbor-

ing gate structures and hence the process window for a subsequent etching or deposition is increased.

[0020] Furthermore, there is no need to etch the liner layer in this invention. Hence, uniformity of the liner layer on the substrate can be ensured and damages to the substrate surface due to over-etching can be avoided.

[0021] In addition, the method for fabricating a contact opening according to this invention is capable of preventing any damage to the substrate surface (the doped region), junction leakage is greatly minimized. Moreover, with damage to the substrate surface reduced, ion implantation for restoring dopant concentration is no longer necessary. In other words, the contact opening fabrication process is very much simplified.

[0022] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF DRAWINGS

[0023] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, to-

gether with the description, serve to explain the principles of the invention.

[0024] Figs. 1A through 1F are schematic cross-sectional views showing the progression of steps for producing a conventional contact opening in a memory device.

[0025] Figs. 2A through 2G are schematic cross-sectional views showing the progression of steps for producing a contact opening according to one preferred embodiment of this invention.

DETAILED DESCRIPTION

[0026] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0027] Figs. 2A through 2G are schematic cross-sectional views showing the progression of steps for producing a contact opening according to one preferred embodiment of this invention. As shown in Fig. 2A, a substrate 100 with a plurality of conductive structures 112 each having a cap layer 110 thereon is provided. In Fig. 2A, the region labeled 102 is the location for forming a bitline contact and

the region labeled 103 is the location having no bitline contact. In other words, the region 102 is a prescribed area within a memory cell region for forming a bitline contact. On the other hand, the region 103 is a prescribed area within a peripheral circuit region or an area within the memory cell region where a bitline contact is not formed.

[0028] In one embodiment of this invention, the conductive structure 112 is a gate structure comprising a gate dielectric layer 104, a polysilicon layer 106 and a metal silicide layer 108, for example. To form the conductive structure 112, a dielectric layer(not show), polysilicon layer(not show), a metal silicide layer(not show) and a silicon nitride layer(not show) are sequentially deposited over the substrate 100. Thereafter, photolithographic and etching processes are carried out to pattern the silicon nitride layer and form a cap layer 110. Using the cap layer 110 as an etching mask, the metal silicide layer and the polysilicon layer are patterned to form the gate structure 112. In the process of patterning the gate structure 112 through an etching operation, a portion of the gate dielectric layer 104 on the substrate 100 will be removed. Hence, overall thickness of the gate dielectric layer 104 is reduced.

[0029] As shown in Fig. 2B, a tilted ion implantation 200 is carried out implanting ions into the sidewalls of the gate structure 112 and sidewalls of the cap layer 110. In the tilted ion implantation 200, the beam of implant ions is set at an angle so that the ions will penetrate the sidewalls of the gate structure 112 and the sidewalls of the cap layer 110 such that no ions penetrate the surface of the substrate 100 and end up within the substrate 100. Hence, it is important that the angle of the implanting ion beam must be set correctly. In other words, if the gap between neighboring gate structure 112 is X and the height of the opening is Y, the smallest tilt angleθ for the tilted ion implantation beam must satisfy the equation $\tan \theta = X/Y$. That is, the tilt angle for carrying out the tilted ion implantation 200 must be greater than the angleθ.

[0030] In one embodiment of this invention, the ionsof tilted ion implantation 200 have the capability to inhibit the growth of an oxide film layer during a thermal oxidation operation. One type of ion having such a capability is nitrogen. In general, the tilted ion implantation 200 is carried out at an energy level between 5 KeV to 15 KeV and an implant dosage between $5E13/cm^2$ to $5E14/cm^2$.

[0031] Aside from implanting ions into the sidewalls of the gate

structures 112 and the cap layer 110 via a tilt angle, a vertical implantation can also be used to implant ions into the substrate to produce equivalent effect of inhibiting the growth of oxide film layer on the sidewall of the gate structures 112 and the cap layer 110.. As shown in Fig. 2C, after steps of Fig. 2A a vertical ion implantation 200a is carried out, during which ions are implanted into the substrate 100 between two neighboring gate structures 112. In the vertical ion implantation 200a, the beam of implant ions aims vertically down so that the ions will penetrate into the substrate 100 between neighboring gate structures 112 only. None of the ions will pass through the sidewalls of the gate structures 112 or the cap layer 110.

[0032] In one embodiment of this invention, the ions used for carrying out the vertical ion implantation 200a have the capability to enhance the growth of an oxide film layer during a thermal oxidation operation. One type of ion having such a capability is oxygen or argon.

[0033] Before or after the tilted ion implantation 200 or the vertical ion implantation 200a, a metal silicide etching operation can be optionally carried out to remove a portion of the sidewalls of the metal silicide layer 108 within the

gate structure 112 and form a structure as shown in Fig. 2D. The etching operation can be carried out using, for example, a RCA1 etching solution. Since the cap layer 110, the polysilicon layer 108 and the gate dielectric layer 104 are resistant to the etching solution, only a portion of the exposed metal silicide sidewall 108 will be removed to produce a recess metal silicide layer 108a.

[0034] The purpose of removing a portion of the metal silicide layer 108 through etching is to prevent crystal overgrowth on the metal silicide layer 108 in a subsequent thermal treatment process that may lead to the production of lateral extrusion. The presence of lateral extrusion on the sidewall of the gate structure 112 often causes undesirable short circuit.

[0035] However, with the implantation of nitrogen ions into the sidewalls of the gate structure 112 and the cap layer 110, the degree of lateral extrusion from the metal silicide layer 108 after a thermal treatment will be reduced. Alternatively, if ions capable of assisting the growth of a silicon oxide film layer are implanted into the substrate 100 between neighboring gate structures 112, overall process time of the thermal treatment can be shortened to reduce the thermal budget. With a lowering of the thermal bud-

get, the extent of lateral extrusion from the metal silicon layer 108 after the thermal treatment is reduced. In other words, the etching operation in Fig. 2D is an optional procedure that may be carried out or not and also can be carried out before or after the tilted ion implantation 200.

[0036] As shown in Fig. 2E, a thermal processing operation is carried out to from a liner layer 202 on the sidewalls of the gate structure 112 and the exposed substrate 100. The liner layer 202 on the sidewalls of the gate structure 112 has a thickness smaller than the liner layer 202 on the substrate 100. Because ions capable of inhibiting the growth of silicon oxide film have already been implanted into the sidewalls of the gate structure 112 or ions capable of enhancing the growth of silicon oxide film have already been implanted into the substrate 100 between two neighboring gate structures 112, the liner layer 202 on the sidewalls of the gate structure 112 will be thinner than the liner layer 202 on the substrate 100 after the thermal processing operation. The thermal processing operation for forming the silicon oxide liner 202 includes, for example, a rapid thermal processing operation followed by a rapid thermal oxidation.

[0037] Because the liner layer 202 on the sidewalls of the gate

structure 112 is thin, there is no need to etch the sidewall oxide layer to increase the gap between neighboring gate structures. Hence, uniformity of the thickness of the liner layer 202 within the regions 102 and 103 are ensured.

[0038] As shown in Fig. 2F, a spacer 118 is formed on each sidewall of the gate structure 112 and the cap layer 110. The spacers 118 are formed, for example, by depositing silicon nitride layer over the substrate 100 and then performing an anisotropic etching on the silicon nitride layer thereafter. Since the liner layer 202 on the substrate 100 is rather thick, the liner layer 202 will hardly be removed completely after the etching operation. In other words, the substrate 100 will not be exposed after the etching operation.

[0039] As shown in Fig. 2G, an insulation layer 120 is formed over the substrate 100. The insulation layer 120 is a silicon oxide layer, for example. Thereafter, the insulation layer 120 is patterned to form a self-aligned contact opening 122 that exposes a portion of the substrate 100 between two neighboring gate structures 112 within the region 102.

[0040] Aside from producing a thinner liner layer 202, the implanted nitrogen ions within the sidewalls of the gate

structure 112 and the cap layer 110 also increases the selectivity between silicon nitride (the cap layer and the spacers) and silicon oxide (the insulation layer) in the etching operation for forming the self-align contact opening.

[0041] Thereafter, metallic material is deposited into the opening 122 to form a contact so that the doped region within the substrate 100 is electrically connected to a subsequently formed bitline.

[0042] This invention utilizes a tilt or a vertical ion implantation to reduce the thickness of the liner layer that is subsequently formed on the sidewall of a gate structure when compared with the liner layer on the substrate surface. Ultimately, a wider gap is produced between neighboring gate structures and hence the process window for a subsequent etching or deposition step is increased.

[0043] In this invention, the liner layer within the regions for forming contact openings as well as some other regions has a uniform thickness. Therefore, the probability of damaging the substrate due to etching through the thin section of a non-uniform liner layer is greatly minimized.

[0044] In addition, the method for fabricating a contact opening according to this invention is capable of preventing any

damage to the substrate surface (the doped region), junction leakage is greatly minimized. Moreover, with damage to the substrate surface reduced, ion implantation for restoring dopant concentration is no longer necessary. The implantation of nitrogen ions into the sidewalls of the gate structure also provides another advantage. The implanted nitrogen ions within the sidewalls of the gate structure 112 and the cap layer 110 increase the etching selectivity between the silicon nitride layer and the silicon oxide layer in the process of forming the self-align contact opening.

[0045] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.